

Sheet 1 of 2

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE
STATEMENT BY APPLICANTS

ATTY. DOCKET NO.
ALT-282APPLN. NO.
10/670,813APPLICANTS
Ramanand Venkata et al.CONF. NO.
7626FILING DATE
September 24, 2003GROUP ART UNIT
2819

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
T	3,473,160	10/1969	Wahlstrom	326	41	
	4,486,739	12/1984	Franaszek et al.	341	59	
	5,689,195	11/1997	Cliff et al.	326	41	
	5,802,103	9/1998	Jeong	375	220	
	5,909,126	6/1999	Cliff et al.	326	41	
	6,031,428	2/2000	Hill	331	11	
	6,215,326	4/2001	Jefferson et al.	326	41	
	6,240,471	5/2001	Schlueter et al.	710	62	
	6,270,350	8/2001	Christopher	434	69	
	6,370,603	4/2002	Silverman	710	72	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

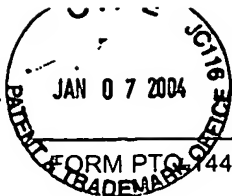
EXAMINER INITIAL	
T	Agere Systems, Inc., "ORCA ORT82G5 0.622/1.0-1.25/2.0-2.5/3.125 Gbits/s Backplane Interface FPSC," Preliminary Data Sheet, pp. 1-35 (July 2001)
T	Agere Systems, Inc., "ORCA ORT8850 Field-Programmable System Chip (FPSC) Eight Channel x 850 Mbits/s Backplane Transceiver," Product Brief, pp. 1-6 (July 2001)
T	Agere Systems, Inc., "ORCA ORT8850 Field-Programmable System Chip (FPSC) Eight Channel x 850 Mbits/s Backplane Transceiver," Product Brief, pp. 1-36 (August 2001)
T	Cook, Barry M., "IEEE 1355 Data-Strobe Links: ATM Speed at RS232 Cost," <u>Microprocessors and Microsystems</u> , vol. 21, no. 7-8, pp. 421-428 (March 30, 1998)
T	Electronic Trend Publications, Inc., "Lucent Introduces 10Gb/s Ethernet FPGAs," <u>Programmable Logic News and Views</u> , vol. 9, no. 11, pp. 7-8 (November 2000)

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DATE CONSIDERED

12/12/05

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicants.



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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
<i>P</i>	6,388,591	5/2002	Ng	341	100	
<i>P</i>	6,407,576	6/2002	Ngai et al.	326	41	
<i>P</i>	2001/0033188 A1	10/2001	Aung et al.	327	41	
<i>P</i>	2002/0190751 A1	12/2002	Lee et al.	326	39	
<i>P</i>	2003/0052709 A1	3/2003	Venkata et al.	326	37	
<i>P</i>	2003/0155955 A1	8/2003	Andrasic et al.	327	277	

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						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
<i>I</i>	Konstas, Jason, "Converting Wide, Parallel Data Buses to High Speed Serial Links," <u>International IC '99 Conference Proceedings</u> , pp. 19-30 (1991)
<i>I</i>	Lemme, Helmuth, "Schnelle Chips Für 'Flaschenhälse'," <u>Elektronik</u> , vol. 40, no. 22, pp. 104-109 (October 29, 1991)
<i>P</i>	Lucent Technologies, Inc., "Protocol Independent Gigabit Backplane Transceiver Using Lucent ORT4622/ORT8850 FPSCs," Application Note, pp. 1-10 (June 2000)
<i>I</i>	Lucent Technologies, Inc., "ORCA ORT82G5 0.622/1.0-1.25/2.0-2.5/3.125 Gbits/s Backplane Interface FPSC," Product Brief, pp. 1-8 (February 2001)
<i>P</i>	Xilinx, Inc., <u>Virtex-II Pro Platform FPGA Handbook</u> (UG012 Version 1.0), pp. 1-6, 27-32, 121-126, and 162-180 (January 31, 2002)
<i>I</i>	Xilinx, Inc., <u>Rocket I/O Transceiver User Guide</u> (UG024 Version 1.2), pp. 1-106 (February 25, 2002)

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